Power Control Chip

rev. PCC170826 (26.8.2017 8:18)

Chip for power control of devices controlled by one button, with one LED indication, with automatic shut down after defined time using Atmel AtTiny85.

Contents

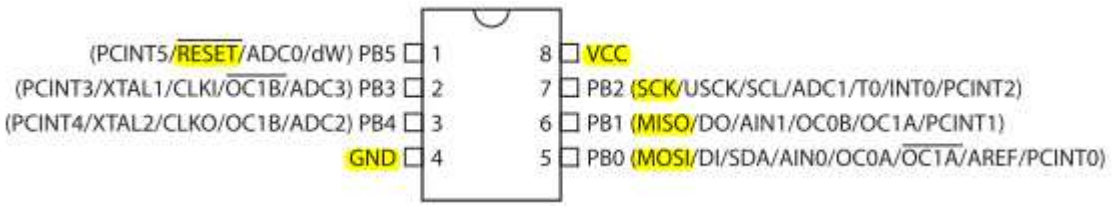
Electrical parameters

Operating voltage 2.7 - 5.5V (for ATtiny25/45/85); Maximum Operating voltage 6.0V

Power consumption at 4V, 128kHz internal oscillator: Active Mode 150uA , idle 80uA, power down 0.4 µA (watch dog disabled)

Voltage on any Pin except RESET with respect to Ground -0.5V to VCC+0.5V; All I/O pins have protection diodes to both VCC and Ground; I/O Pin Pull-up Resistor 20 to 50 kohm; max. I/O DC current 40mA

Power consumption: ON .. 270uA at 2,5V, 440uA at 5,0V; OFF .. <1uA at 2,5V, <2uA at 5,0V



Pin description

\ = negative

pin	port	name	pin type	description
1	PB5	Reset	input	H = turn off (eg. for overcurrent guard); normally must be held L!
2	PB3	Amp_Out	output	H = amplifier on, L = off
3	PB4	Off_Out	output	H = turned off (= \On_Out) / dw at Debug
4	GND	GND		
5	PB0	\Led_Out	output	LED output 40mA, common anode (lights on L)
6	PB1	On_In	input	module on/off signal (external power down just for amplifier); normally must be held H
7	PB2	\Btn_In	input	control button to GND
8	VCC	VCC		

(green = changed in comparsion to previous version)

Function

control

button - short push: 0,1-2,5s, long push: 2,5-6s

to turn on in off mode – short on long push

to turn off in on mode – short push or wait for sleep time

to go into programming in on mode – long push

to leave programming mode – long push or wait for 5s

to change sleep time in programming mode – short push to change to 1 – 2 - ... 7x 20min for –L version (or 20s for –S version) or steady (not turning off) (indicated by 8 flashing – just for L version)

indication by LED

off = turn off

on = turn on

in program mode

- length of sleep time by number of short flashes at entering the programming mode or after changing the sleep time by short button pressing
- long flash (1s) at leaving the mode
- shot flashing after change

sleep mode (On_in = H) – long flashing of LED (5s turn off, 0.1s turn on)

low power voltage

- <2,9V – 2 short flashes every 2 sec
- <3,4V – 1 short flash every 2 sec

Driving

in sleep mode – Amp_out = L, Off_out = L

in on mode - Amp_out = H, Off_out = L

in off mode - Amp_out = L, Off_out = H

Overview

H, L, x = does not matter, p = previous state, n = time of power on in time units

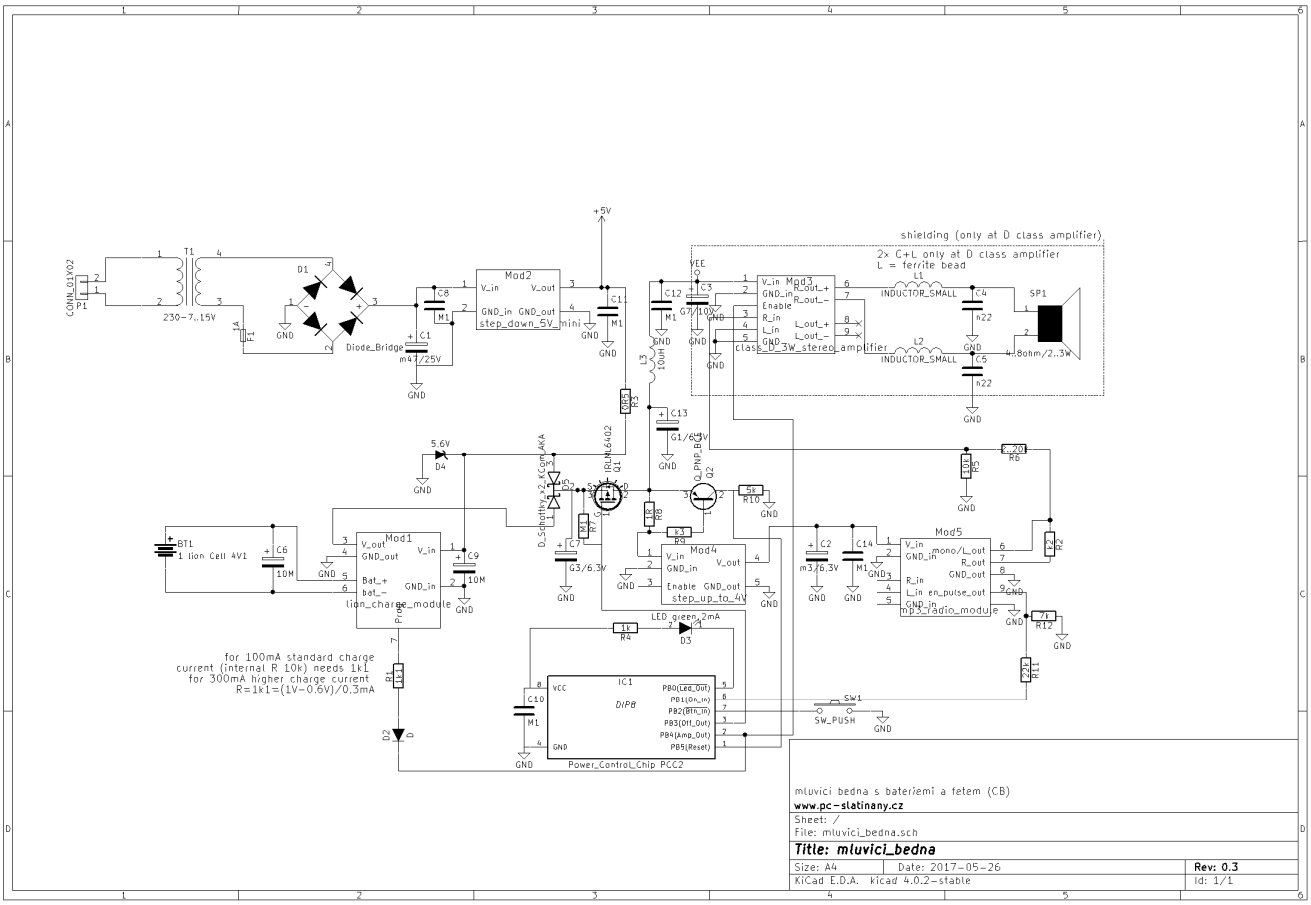
mode before	**responds to**		**mode after**	**\Led_Out**	**On_Out**	**Amp_Out**	**PortOutByte PortB543210**	**rem.**
off	**\Btn_In**	HLH L<5s	**on**	HLLHLHL (N x H)	LH	LH	0b011110	long or short pressing of button
on prog idle	**\Btn_In**	HLH L<2s	**off**	HL	HL	HL	0b100111	long or short pressing of button
on	**\Btn_In**	HLLH L>2s	**prog**	LHLHL (N x H)	p (H)	p (H or L)	see on	long pressing of button
prog	**\Btn_In**	H>10s	**on**	HLH	p (H)	p (H or L)	see on	button not pressed for 10s leaves prog mode
prog	**\Btn_In**	HLLH L>2s	**prog**	LHLHL (N+1 x H)	p (H)	p (H or L)	see on	long pressing of button
on prog	**On_In**	HL	**idle**	LHHLHHL	p (H)	HL	0b010111	module stays on, amplifier off (LED flashes shortly every 2sec.)
idle	**On_In**	LH	**on**	LHLHL (N x H)	p (H)	LH	see on	module turned on – turns on amplifier and resets power off timer (like at power on)
off	supply	LH	**off**	HLH	L	L	see off	after supply on, when before was turned off normally (either by button or timer) – LED flashes 1x
off	supply	LH	**off**	HLHHLHH (N=4)	L	L	see off	after supply on, when before was turned off abnormally (neither by button nor timer) – LED flashes 4x

Modes: **on** = power on; **prog** = programming of time of power on; **off** = power off; **idle** = power on, but amplifier off

Led_Out = LED connected with cathode (lights on L)

Example application

MP3 player



Remarks:

- the amplifier is connected to battery charger to limit current consumption at mains power to prevent overloading step down converter
- battery charger current should be adjusted not to damage battery, but to be enough for supply the amplifier – e.g. 400mA at power off and 900mA at power on (increasing of the current done by R1)

Firmware Codes

PCC-S 170826	-S = short time (1-8x20s); -L = long time (1-8x20min or steady) revision of the program: yymmdd	pin nr. 1 on left bottom (close to yy)

Remarks to the program used

(not intended for end user)

Fuses

AtTiny85(45) – used fuses:

- SUT_CKSEL =1 -128kHz clock – WD.osc. 128kHz
- BODLEVEL = 0 - BOD disable (if enabled, consumes 20uA in off state, instead <1uA)
- RSTDISBL = 1 - B5 enable (instead of reset)

DebugWire

When the debugWIRE Enable (DWEN) Fuse is programmed (default is 1 = uprogrammed) and Lock bits are unprogrammed, the debugWIRE system within the target device is activated.

Pull-Up resistor on the dW/(RESET) line must be in the range of 10k to 20 k□. However, the pull-up resistor is optional.

A programmed DWEN Fuse enables some parts of the clock system to be running in all sleep modes. This will increase the power consumption while in sleep. Thus, the DWEN Fuse should be disabled when debugWire is not used.

The debugWIRE interface is asynchronous, which means that the debugger needs to synchronize to the system clock. If the system clock is changed by software (e.g. by writing CLKPS bits) communication via debugWIRE may fail. Clock frequencies below 100kHz may cause communication problems.

To disable the debugWIRE interface, use high-voltage programming to unprogram the DWEN fuse. Alternately, use the debugWIRE interface to disable temporarily itself, which will allow SPI programming to take place, provided that the SPIEN fuse is set.

Interrupts

The contents of the Register File and SRAM are unaltered when the device wakes up from sleep. (p.34)

Wake up from Power-down

For INT0 (PB2), only level interrupt. (p.34)

in Power-down mode to avoid high power consumption if some input signals are left floating, or have an analog signal level close to VCC/2. (p.56)

9.2.1 Low Level Interrupt

A low level interrupt on INT0 (PB2) is detected asynchronously. This implies that this interrupt can be used for waking the part also from sleep modes other than Idle mode. The I/O clock is halted in all sleep modes except Idle mode. Note that if a level triggered interrupt is used for wake-up from Power-down, the required level must be held long enough for the MCU to complete the wake-up to trigger the level interrupt. If the level disappears before the end of the Start-up Time, the MCU will still wake up, but no interrupt will be generated. The start-up time is defined by the SUT and CKSEL Fuses as described in “System Clock and Clock Options” on page 23. If the low level on the interrupt pin is removed before the device has woken up then program execution will not be diverted to the interrupt service routine but continue from the instruction following the SLEEP command. (p.49)

configuration

INT0

MCUCR 0x35 – MCU Control Register: ISC01 (b1) ISC00 (b0)= 0 0 The low level of INT0 generates an interrupt request.

GIMSK 0x3B – General Interrupt Mask Register: INT0 (b6) When the INT0 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), the external pin interrupt is enabled.

pin change

GIMSK – General Interrupt Mask Register: When the PCIE bit (b5) is set (one) and the I-bit in the Status Register (SREG) is set (one), pin change interrupt is enabled. Any change on any enabled PCINT[5:0] pin will cause an interrupt.

PCMSK – Pin Change Mask Register : PCINT0 (b0) ... PCINT5 (b5)

Counters

12-Bit Timer/Counter Combining the 4-bit USI counter with one of the 8-bit timer/counters creates a 12-bit counter. (p.114)

Note that even when no wire mode is selected (USIWM[1:0] = 0) the external clock input (USCK/SCL) can still be used by the counter. (p.116)

USISR – USI Status Register (0x0E) •

Bit 6 – USIOIF: Counter Overflow Interrupt Flag - This flag is set (one) when the 4-bit counter overflows (i.e., at the transition from 15 to 0) - A counter overflow interrupt will wakeup the processor from Idle sleep mode. The flag will only be cleared if a one is written to the USIOIF bit.

Bits 3:0 – USICNT[3:0]: Counter Value

USICR – USI Control Register (0x0D)

• Bit 6 – USIOIE: Counter Overflow Interrupt Enable Setting this bit to one enables the counter overflow interrupt. If is there a pending interrupt and USIOIE and the Global Interrupt Enable Flag are set to one the interrupt will be executed immediately. (p.116)

Bits 5:4 – USIWM[1:0]: Wire Mode = 0 0: Outputs, clock hold, and start detector disabled. Port pins operates as normal.

Bits 3:2 – USICS[1:0]: Clock Source Select = 0 1: Timer/Counter0 Compare Match Timer/Counter0 Compare Match

WDT

To turn WDT on:

To turn WDT off:

To disable an enabled Watchdog Timer, the following procedure must be followed:

1. In the same operation, write a logic one to WDCE (0x21.4) and WDE (0x21.3) (of WDTCR). A logic one must be written to WDE even

however, it is set to one before the disable operation starts.

2. Within the next four clock cycles, write logic 0 to WDE (0x21.3). This disables the Watchdog.

Pins

Port Pin Configurations (p.55)

In with pull up: DDxn=0, PORTxn=1, PUD (in MCUCR)=0

In high Z: DDxn=0, PORTxn=1, PUD (b6 in MCUCR)=1 or DDxn=0, PORTxn=0, PUD (b6 in MCUCR)=x

Out: DDxn=1, PORTxn=0/1, PUD (b6 in MCUCR)=X

Reset pin

• Port B, Bit 5 – RESET/dW/ADC0/PCINT5:

1. RESET: External Reset input is active low and enabled by unprograming (“1”) the RSTDISBL Fuse. - ! both ISP and debugwire disabled, just parallel programming
2. dW: When the debugWIRE Enable (DWEN) Fuse is programmed and Lock bits are unprogrammed, the debugWIRE system within the target device is activated. The RESET port pin is configured as a wire-AND (open-drain) bi-directional I/O pin with pull-up enabled and becomes the communication gateway between target and emulator.

Analog to Digital Converter (p.122)

0 – VCC ADC Input Voltage Range; Selectable 1.1V / 2.56V ADC Voltage Reference

VBG Bandgap reference voltage V CC = 5.5V TA= 25°C 1.0 - 1.1 - 1.2 V (p.165)

problem: when IE (interrupt enabled), irq was called repeatedly without start by the bit

Fuses

Internal 128 kHz Oscillator

SUT[1:0]=10 ... Start-up Time from Power-down 6 CK; Delay from Reset: 14CK + 64 ms Slowly rising power

System Clock Prescaler

The ATtiny25/45/85 system clock can be divided by setting the “CLKPR – Clock Prescale Register” on page 32. This feature can be used to decrease power consumption when the requirement for processing power is low.

• Bits 3:0 – CLKPS[3:0]: Clock Prescaler Select Bits 3 – 0 CLKPS3 CLKPS2 CLKPS1 CLKPS0:

0 0 0 0 division factor 1; 1 0 0 0 division factor 256

Power-down Mode

When the SM[1:0] bits are written to 10, the SLEEP instruction makes the MCU enter Power-down mode.

Program flow-chart